COMPLETE LISTING OF CLAIMS

1-17 (Cancelled)

18. (New) A chip capacitor comprising:

a multilayer body including a plurality of stacked ceramic sheet layers;

a plurality of inner electrodes disposed within the multilayer body;

a plurality of connectors disposed within the multilayer body so as to electrically connect the plurality of inner electrodes to each other; and

a plurality of strip electrodes formed on outer main surfaces of the multilayer body and electrically connected to some of the inner electrodes via corresponding connectors of the plurality of connectors,

wherein a surface in a longitudinal direction of the multilayer body is a mounting surface of the chip capacitor for mounting on a printed circuit board.

19. (New) The chip capacitor according to claim 18, wherein each connector of the plurality of connectors includes an aperture extending between the outer main surfaces, the aperture substantially being filled with a conductive material.

20. (New) The chip capacitor according to claim 18, wherein different connectors of the plurality of connectors electrically couple adjacent inner electrodes to each other.

21. (New) The chip capacitor according to claim 18, wherein at least one of the inner electrodes is in the form of a strip line.

22. (New) A manufacturing method for a chip capacitor, the method comprising:

preparing a plurality of ceramic mother sheet layers;

forming a plurality of inner electrodes and connectors in some of the

plurality of ceramic mother sheet layers;

forming a mother multilayer body by stacking the plurality of mother sheet layers and press-bonding them together;

forming a plurality of strip electrodes on outer main surfaces of the mother multilayer body, the strip electrodes being electrically connected to some of the inner electrodes via corresponding connectors of the plurality of connectors;

cutting the mother multilayer body into separate multilayer bodies, each separate multilayer body including the inner electrodes, the strip electrodes, and the connectors; and

firing one of the mother multilayer body and the separate multilayer bodies.

23. (New) The method of manufacturing a chip capacitor according to claim 22, wherein the connectors are formed in the ceramic mother layer sheets by forming an aperture between the outer main surfaces and substantially filling the aperture with a conductive material.

24. (New) The method of manufacturing a chip capacitor according to claim 22, wherein the connectors are formed such that different connectors of the plurality of connectors electrically couple adjacent inner electrodes to each other.

25. (New) The method of manufacturing a chip capacitor according to claim 22, wherein at least one of the inner electrodes is formed as a strip line.